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(pipelined loop)

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Journal or Magazine = **JNL** Conference = **CNF** Standard = **STD**

1 Software pipelining loops with conditional branches

Stoodley, M.G.; Lee, C.G.;

Microarchitecture, 1996. MICRO-29. Proceedings of the 29th Annual IEEE/ACM International Symposium on , 2-4 Dec. 1996

Page(s): 262 -273

[\[Abstract\]](#) [\[PDF Full-Text \(1260 KB\)\]](#) **IEEE CNF**

2 Optimal code size reduction for software-pipelined loops on DSP applications

Qingfeng Zhuge; Zili Shao; Sha, E.H.-M.;

Parallel Processing, 2002. Proceedings. International Conference on , 18-21 Aug. 2002

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[\[Abstract\]](#) [\[PDF Full-Text \(330 KB\)\]](#) **IEEE CNF**

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Govindarajan, R.; Altman, E.R.; Gao, G.R.;

Parallel and Distributed Systems, IEEE Transactions on , Volume: 7 Issue: 11 , Nov. 1996

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[\[Abstract\]](#) [\[PDF Full-Text \(1684 KB\)\]](#) **IEEE JNL**

4 Evaluating the use of register queues in software pipelined

loops

Tyson, G.S.; Smelyanskiy, M.; Davidson, E.S.;

Computers, IEEE Transactions on , Volume: 50 Issue: 8 , Aug. 2001

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Llosa, J.; Valero, M.; Ayguade, E.;

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8 An evaluation of fine-grain producer-initiated communication in cache-coherent multiprocessors

Abdel-Shafi, H.; Hall, J.; Adve, S.V.; Adve, V.S.;

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11 Register queues: a new hardware/software approach to efficient software pipelining

Smelyanskiy, M.; Tyson, G.S.; Davidson, E.S.;

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14 Optimum and heuristic data path scheduling under resource constraints

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